Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method for upgrading firmware in an embedded system, comprising the steps of:

providing a processor;

providing a non-volatile programmable read only memory device having a fixed vector table, a boot area for storing boot code, a first application area for storing firmware, and a second application area for storing firmware;

providing a random access memory device (RAM) having a software vector table and a RAM application area;

programming the fixed vector table with a reset vector address and interrupt vector addresses, said reset vector address pointing to the boot code in said boot area and said interrupt vector addresses pointing to corresponding interrupt vector addresses in the software vector table;

loading an upgraded version of firmware into one of the first application area or the second application area;

resetting the processor to run the upgraded version of firmware; and

filling the software vector table with proper corresponding interrupt vector addresses for the interrupt vectors contained in the fixed vector table as determined by the upgraded version of firmware;

wherein:

in the event an interrupt is generated, the processor obtains a next instruction from one of the interrupt vector addresses of the fixed vector table in accordance with said interrupt;

said next instruction points to a corresponding location in the software vector table; and

said corresponding location in the software vector table points to a corresponding location in one of said first or second application areas.

2. (Original) A method in accordance with claim 1, wherein the non-volatile programmable read only memory device comprises a flash electrically erasable programmable read only memory device (FLASH).

3. (Original) A method in accordance with claim 1, wherein a prior version of firmware is running from one application area while the upgraded version of firmware is being loaded into the other application area.

4. (Original) A method in accordance with claim 1, further comprising:

providing an erasable programmable memory device (EPROM) which is used to determine which application area will be accessed after the resetting step.

5. (Original) A method in accordance with claim 1, further comprising:
loading the RAM application area with data from the
application area having the upgraded version of firmware.

6. (Original) A method in accordance with claim 1, wherein:

the first application area contains a first version of firmware; and

the second application area contains a second version of firmware.

7. (Original) A method in accordance with claim 1, wherein said processor, said non-volatile programmable read only memory device, and said RAM are all provided in the form of a single integrated circuit.

8. (Currently amended) An upgradable embedded system apparatus, comprising:

a processor;

a non-volatile programmable read only memory device having a fixed vector table, a boot area for storing boot code, a first application area for storing firmware, and a second application area for storing firmware; and

a random access memory device (RAM) having a software vector table and a RAM application area;

wherein:

the fixed vector table is programmed with a reset vector address and interrupt vector addresses, said reset vector address pointing to the boot code in said boot area and said interrupt vector addresses pointing to corresponding interrupt vector addresses in the software vector table;

an upgraded version of firmware is loaded into one of the first application area or the second application area;

the processor is reset to run the upgraded version of firmware; ~~and~~

the software vector table is filled with proper corresponding interrupt vector addresses for the interrupt vectors contained in the fixed vector table as determined by the upgraded version of firmware ;

in the event an interrupt is generated, the processor obtains a next instruction from one of the interrupt vector addresses of the fixed vector table in accordance with said interrupt;

said next instruction points to a corresponding location in the software vector table; and

said corresponding location in the software vector table points to a corresponding location in one of said first or second application areas.

9. (Original) Apparatus in accordance with claim 8, wherein the non-volatile programmable read only memory device comprises a flash electrically erasable programmable read only memory device (FLASH).

10. (Original) Apparatus in accordance with claim 8, wherein a prior version of firmware is running from the one application area while the upgraded version of firmware is being loaded into the other application area.

11. (Original) Apparatus in accordance with claim 8, further comprising:

an erasable programmable memory device (EPROM) which is used to determine which application area will be accessed after the resetting step.

12. (Original) Apparatus in accordance with claim 8, wherein:
the RAM application area is loaded with data from the
application area having the upgraded version of firmware.

13. (Original) Apparatus in accordance with claim 8, wherein:

the first application area contains a first version of firmware; and

the second application area contains a second version of firmware.

14. (Original) Apparatus in accordance with claim 8, wherein said processor, said non-volatile programmable read only memory device, and said RAM are all provided in the form of a single integrated circuit.